REMARKS

Reconsideration of this application as amended is respectfully requested. Claims 22, 46-48, 59, 68 and 69 have been canceled without prejudice, claim 57 has been amended, and new claim 70 has been added. No new matter has been added. Claims 1-21, 23-45, 49-58, 60-67, and 70 are pending. The remarks below refer to the claims as amended herein.

Claim Rejections -- Double Patenting

Claims 21, 35, 41, 49, 57 and 64 have been provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,728,124. Applicant has enclosed a Terminal Disclaimer in compliance with 37 CFR 1.321(c) to overcome the obviousness-type double-patenting rejection.

Claim Rejections - 35 U.S.C. § 112

Claim 22 has been rejected under 35 U.S.C. § 112, second paragraph as being indefinite because it depends from higher-numbered claim 23. To overcome this reason for rejection, applicant has canceled claim 22 and reinserted its contents verbatim in a new claim 70.

Claim Rejections -- 35 U.S.C. § 103

Claims 1-2, 11-13, 16, 18-21, 27, 35, 41, 49, 57 and 64 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,154,384 to Nataraj et al. ("Nataraj") in view of U.S. Patent 6,014,755 to Wells et al. ("Wells").

Claim 1 recites in part:

> an error detection circuit coupled to receive, via the bit lines, a selected data word from one of the rows of CAM cells and to determine, concurrently with the compare operation, whether the selected data word includes an error.

Nataraj discloses a TCAM device wherein comparand data is provided on compare signal lines and that read and write data is carried on data bit lines (Nataraj, col. 2 lines 47-49). Wells suggests a method of operating a flash memory device wherein, in

response to a read operation, data from an entire sector of memory may be read and then transferred to an error detection circuit, which may then detect whether an error has occurred (Wells, col. 9 lines 24-53). Neither Nataraj nor Wells discloses "an error detection circuit coupled to receive, via the bit lines, a selected data word from one of the rows of CAM cells and to determine, *concurrently with the compare operation*, whether a selected data word includes an error", as recited in claim 1. Accordingly, even if Nataraj and Wells could be combined in the manner proposed in the Office Action, the combination would still lack at least the above-recited limitation of claim 1 and therefore would not have rendered claim 1, nor dependent claims 2, and 11-13, obvious.

Claim 16 recites in part:

> a second circuit responsive to an error indication from the first circuit, to output an error signal if the selected data word is determined to include an error, the second circuit including an input to receive the validity value that corresponds to the selected data word and being adapted to prevent assertion of the error signal if the validity value indicates that the selected data word is not a valid data word.

Applicant submits that neither Nataraj nor Wells discloses or suggests a circuit to output an error signal if a selected data word is determined to include an error and being adapted to prevent assertion of the error signal if a validity value indicates that the selected data word is not a valid data word, as recited in claim 16. Thus, even if Nataraj and Wells could be combined in the manner proposed in the Office Action, the combination would still lack at least the above-recited limitation of claim 16 and therefore would not have rendered claim 16, nor dependent claims 18-20 obvious.

Claim 21 recites in part:

> an error detection circuit coupled to the CAM array to receive a data word from a selected one of the rows of CAM cells and to receive a corresponding validity value from one of the validity storage cells.

Applicant submits that neither Nataraj nor Wells discloses or suggests the above-

recited limitation of claim 21, nor is any such disclosure pointed out in the Office Action. Thus, even if Nataraj and Wells could be combined in the manner suggested in the Office Action, the combination still would lack at least the above-recited element and therefore would not have rendered claim 21 obvious.

Claim 27 recites in part:

> an address generator to output a plurality of error check addresses in a predetermined sequence;

Applicant submits that neither Nataraj nor Wells discloses or suggests the above-recited limitation of claim 27, nor is any such disclosure pointed out in the Office Action. Thus, even if Nataraj and Wells could be combined in the manner suggested in the Office Action, the combination still would lack at least the above-recited element and therefore would not have rendered claim 27 obvious.

Claim 35 recites in part:

> determining, concurrently with the compare operation, whether a selected data word of the plurality of data words includes an error, wherein said determining includes outputting the selected data word from the CAM array.

Applicant submits that, at least for the reasons given with respect to claim 1, even if Nataraj and Wells could be combined in the manner proposed in the Office Action, the combination would still lack at least the above-recited limitation and therefore would not have rendered claim 35 obvious.

Claim 41 recites in part:

> asserting an error signal if the selected data word is determined to include an error and if a validity value that corresponds to the selected data word indicates that the selected data word is a valid data word.

Applicant submits that, at least for the reasons given with respect to claim 16, even if Nataraj and Wells could be combined in the manner proposed in the Office Action, the combination would still lack the above-recited limitation and therefore would

not have rendered claim 41 obvious.

Claim 49 recites in part:

> A CAM device coupled to the plurality of signal lines, the CAM device including an error checking circuit to automatically check, in order according to address, each of a plurality of data values stored within the CAM device for error and to signal the processor via one or more of the plurality of signal lines in response to detecting an error in any one of the plurality of data values.

As discussed above, Wells suggests a method of operating a flash memory device wherein an error checking process begins at a first step at which an attempt is made to read data from a sector (Wells, col. 9 lines 39-47). As such, Wells discloses a method of error-checking which occurs at a particular memory location in response to a data read operation, and not a "CAM device including an error checking circuit to automatically check, in order according to address, each of a plurality of data values stored within the CAM device for error", as recited in claim 49. Because Nataraj also does not disclose the above-recited limitation, even if Nataraj and Wells could be combined in the manner proposed in the Office Action, the combination would still lack at least the above-recited limitation and therefore would not have rendered claim 49 obvious.

Claim 57 recites in part:

> a CAM array including a plurality of CAM cells for storing a plurality of data words, the CAM array further including a plurality of validity storage cells for storing a plurality of validity values associated with the plurality of data words

Applicant submits that neither Nataraj nor Wells discloses or suggests the above-recited limitation of claim 57, nor is any such disclosure pointed out in the Office Action. Thus, even if Nataraj and Wells could be combined in the manner suggested in the Office Action, the combination still would lack at least the above-recited element and therefore would not have rendered claim 57 obvious.

Claim 64 recites in part:

> means for concurrently (i) determining whether a data word stored in a selected row of the CAM cells has an error, including outputting the data word from the selected row of CAM cells; and (ii) comparing comparand data with the data words.

Applicant submits that, at least for the reasons given with respect to claim 1, even if Nataraj and Wells could be combined in the manner proposed in the Office Action, the combination would still lack at least the above-recited limitation and therefore would not have rendered claim 64 obvious.

Claims 3-10, 14-15, 17, 22-26, 28-34, 36-40, 42-45, 50-56, 58-63 and 65-67 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,154,384 to Nataraj et al. ("Nataraj") in view of U.S. Patent 6,014,755 to Wells et al. ("Wells"), and further in view of U.S. Patent 6,067,656 to Rusu et al. ("Rusu").

Claims 3-10 and 14-15 depend from claim 1 and therefore include the following limitation:

> an error detection circuit coupled to receive, via the bit lines, a selected data word from one of the rows of CAM cells and to determine, concurrently with the compare operation, whether the selected data word includes an error.

As discussed above in reference to claim 1, neither Nataraj nor Wells disclose the above-recited limitation. Rusu discloses a method for detecting soft errors in CAM arrays wherein, as the flowchart of Figure 4C of Rusu illustrates, an input signal is first compared to tag words stored in a CAM array for a match. An output signal is then sent from the CAM array to a parity comparator in response to finding a match between the input data signal and a particular tag word stored in the CAM array (Rusu, col. 5 lines 47-55). Like Nataraj and Wells, however, Rusu does not disclose or suggest "an error detection circuit coupled to receive, via the bit lines, a selected data word from one of the rows of CAM cells and to determine, *concurrently with the compare operation*, whether a selected data word includes an error", as recited in claim 1. Accordingly, even if Nataraj, Wells, and Rusu could be combined in the manner suggested in the Office Action, the

combination would still lack at least the above-recited limitation and therefore would not have rendered claims 3-10 or 14-15 obvious.

Claim 17 depends from claim 16 and therefore includes the following limitation:

> a second circuit responsive to an error indication from the first circuit, to output an error signal if the selected data word is determined to include an error, the second circuit including an input to receive the validity value that corresponds to the selected data word and being adapted to prevent assertion of the error signal if the validity value indicates that the selected data word is not a valid data word.

As discussed above in reference to claim 16, neither Nataraj nor Wells discloses the above-recited limitation, and applicant submits that Rusu also does not disclose the above-recited limitation. Rusu further discloses a parity comparator circuit which compares the original parity of a particular tag word stored in the CAM array with the parity signal received from the parity encoder to generate a "hit" signal, indicative of whether the tag word contains an error, depending whether the two parities match (Rusu, col. 5 line 57 to col. 6 line 3). However, Rusu does not disclose or suggest a circuit to output an error signal if a selected data word is determined to include an error and being adapted to prevent assertion of the error signal if a validity value indicates that the selected data word is not a valid data word, as recited in claim 16. Accordingly, even if Nataraj, Wells, and Rusu could be combined in the manner suggested in the Office Action, the combination would still lack at least the above-recited limitation and therefore would not have rendered claim 17 obvious.

Claims 22-26 depend from claim 21 and therefore include the following limitation:

> an error detection circuit coupled to the CAM array to receive a data word from a selected one of the rows of CAM cells and to receive a corresponding validity value from one of the validity storage cells.

As discussed above in reference to claim 21, neither Nataraj nor Wells discloses the above-recited limitation, and applicant submits that Rusu also does not disclose the above-recited limitation. Accordingly, even if Nataraj, Wells, and Rusu could be combined in the manner suggested in the Office Action, the combination would still lack at least the above-recited limitation and therefore would not have rendered claims 22-26 obvious.

Claims 28-34 depend from claim 27 and therefore include the following limitation:

> an address generator to output a plurality of error check addresses in a predetermined sequence;

As discussed above in reference to claim 27, neither Nataraj nor Wells discloses the above-recited limitation, and applicant submits that Rusu also does not disclose the above-recited limitation. Accordingly, even if Nataraj, Wells, and Rusu could be combined in the manner suggested in the Office Action, the combination would still lack at least the above-recited limitation and therefore would not have rendered claims 28-34 obvious.

Claims 36-40 depend from claim 35 and therefore include the following limitation:

> determining, concurrently with the compare operation, whether a selected data word of the plurality of data words includes an error, wherein said determining includes outputting the selected data word from the CAM array.

As discussed above in reference to claim 35, neither Nataraj nor Wells discloses the above-recited limitation, and applicant submits that Rusu also does not disclose the above-recited limitation. Accordingly, even if Nataraj, Wells, and Rusu could be combined in the manner suggested in the Office Action, the combination would still lack at least the above-recited limitation and therefore would not have rendered claims 36-40 obvious.

Claims 42-45 depend from claim 41 and therefore include the following

limitation:

> asserting an error signal if the selected data word is determined to include an error and if a validity value that corresponds to the selected data word indicates that the selected data word is a valid data word.

As discussed above in reference to claim 41, neither Nataraj nor Wells discloses the above-recited limitation, and applicant submits that Rusu also does not disclose the above-recited limitation. Accordingly, even if Nataraj, Wells, and Rusu could be combined in the manner suggested in the Office Action, the combination would still lack at least the above-recited limitation and therefore would not have rendered claims 42-45 obvious.

Claims 50-56 depend from claim 49 and therefore include the following limitation:

> A CAM device coupled to the plurality of signal lines, the CAM device including an error checking circuit to automatically check, in order according to address, each of a plurality of data values stored within the CAM device for error and to signal the processor via one or more of the plurality of signal lines in response to detecting an error in any one of the plurality of data values.

As discussed above in reference to claim 49, neither Nataraj nor Wells discloses the above-recited limitation, and applicant submits that Rusu also does not disclose the above-recited limitation. Rusu discloses an error-checking process initiated after an input signal is compared to tag words stored in a CAM array for a match (Rusu, col. 5 lines 47-51). As such, Rusu discloses a process of error-checking which occurs at a particular memory location in response to a compare operation, and not a "CAM device including an error checking circuit to automatically check, in order according to address, each of a plurality of data values stored within the CAM device for error", as recited in claim 49. Accordingly, even if Nataraj, Wells, and Rusu could be combined in the manner proposed in the Office Action, the combination would still lack at least the above-recited

limitation and therefore would not have rendered claims 50-56 obvious.

Claims 58-63 depend from claim 57 and therefore include the following limitation:

> a CAM array including a plurality of CAM cells for storing a plurality of data words, the CAM array further including a plurality of validity storage cells for storing a plurality of validity values associated with the plurality of data words

As discussed above in reference to claim 57, neither Nataraj nor Wells discloses the above-recited limitation, and applicant submits that Rusu also does not disclose the above-recited limitation. Rusu discloses a CAM array for storing tag words, and a separate parity comparator circuit for storing the original parity of an associated tag word stored in the CAM array (Rusu, col. 4 line 64 to col. 5 line 4). Rusu neither discloses nor suggests "a CAM array including a plurality of CAM cells for storing a plurality of data words, the CAM array further including a plurality of validity storage cells for storing a plurality of validity values associated with the plurality of validity values associated with the plurality of data words", as recited in claim 57. Accordingly, even if Nataraj, Wells, and Rusu could be combined in the manner proposed in the Office Action, the combination would still lack at least the above-recited limitation and therefore would not have rendered claims 58-63 obvious.

Claims 65-67 depend from claim 64 and therefore include the following limitation:

> means for concurrently (i) determining whether a data word stored in a selected row of the CAM cells has an error, including outputting the data word from the selected row of CAM cells; and (ii) comparing comparand data with the data words.

As discussed above in reference to claim 64, neither Nataraj nor Wells discloses the above-recited limitation, and applicant submits that Rusu also does not disclose the above-recited limitation. Accordingly, even if Nataraj, Wells, and Rusu could be

combined in the manner suggested in the Office Action, the combination would still lack at least the above-recited limitation and therefore would not have rendered claims 65-67 obvious.

In Conclusion

Applicant respectfully submits that all pending claims are in condition for allowance. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

Applicant hereby petitions for an extension of time and authorizes deposit account 501914 to be charged for the fee due in connection with such petition.

Respectfully submitted,

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